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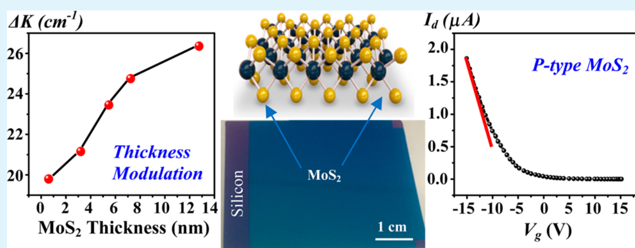
Growth of Large-Scale and Thickness-Modulated MoS_2 Nanosheets

Nitin Choudhary,[†] Juhong Park,[†] Jun Yeon Hwang,[‡] and Wonbong Choi*[,†]

[†]Department of Materials Science and Engineering, University of North Texas, Denton, Texas 76207, United States

[‡]Carbon Convergence Materials Research Center, Korea Institute of Science and Technology, Jeonbuk, 565-905, South Korea

ABSTRACT: Two-dimensional MoS_2 is a promising material for next-generation electronic and optoelectronic devices due to its unique electrical and optical properties including the band gap modulation with film thickness. Although MoS_2 has shown excellent properties, wafer-scale production with layer control from single to few layers has yet to be demonstrated. The present study explored the large-scale and thickness-modulated growth of atomically thin MoS_2 on Si/SiO_2 substrates using a two-step sputtering−CVD method. Our process exhibited wafer-scale fabrication and successful thickness modulation of MoS_2 layers from monolayer (0.72 nm) to multilayer (12.69 nm) with high uniformity. Electrical measurements on MoS_2 field effect transistors (FETs) revealed a *p*-type semiconductor behavior with much higher field effect mobility and current on/off ratio as compared to previously reported CVD grown MoS_2-FETs and amorphous silicon (a-Si) thin film transistors. Our results show that sputter−CVD is a viable method to synthesize large-area, high-quality, and layer-controlled MoS_2 that can be adapted in conventional Si-based microfabrication technology and future flexible, high-temperature, and radiation hard electronics/optoelectronics.



KEYWORDS: *MoS_2, PVD-CVD, thin films, field effect transistors*

1. INTRODUCTION

In recent years, 2D materials like graphene and transition-metal dichalcogenides (TMDs) are gaining a wealth of attention from the scientific community and industry for being the promising materials for next-generation ultrathin electronic and optoelectronic devices.[1−3] The most interesting feature of these materials is that the bulk of these materials are composed of layered structures with strong covalent bonding within each layer and weak van der Waals forces between the adjacent layers. Therefore, single- or few-layer nanosheets of these materials can be obtained by using mechanical exfoliation using adhesive tapes.[4] Graphene is fundamentally and technologically interesting for a variety of applications with remarkable electronic properties; e.g., its massless Dirac fermions have an effective speed of light $v_F \approx 10^6$ ms^{-1} and a room temperature mobility of 200,000 cm^2 V^{-1} s^{-1} in addition to its flexibility and high transparency.[5] However, the absence of a band gap in graphene leading to a very low $I_{on/off}$ ratio limits its broader use for applications in electronics such as logic devices.[6] With this consideration, TMDs, in particular, molybdenum disulfide (MoS_2), have recently emerged as a great alternative to graphene that offers a better solution of fabricating high-performance electronic devices as they are intrinsic semiconductors and possesses unique properties of quantum confinement and thickness-dependent band gap, i.e., changing from 1.3 to 1.9 eV for bulk (indirect band gap) and single-layer (direct band gap) MoS_2, respectively.[7,8] Therefore, MoS_2 could complement graphene and find its unique applications in flexible electronics, high-temperature, and radiation hard electric and optoelectric devices. There have been several efforts in fabricating single-layer (SL) MoS_2 using a mechanical exfoliation method, but a low value of mobility on SiO_2 substrates typically 0.01−10 cm^2 V^{-1} s^{-1} was found.[7,9] Wang et al.[10] studied mechanically exfoliated MoS_2 on SiO_2 and found the room-temperature mobility of ∼10 cm^2 V^{-1} s^{-1} for bilayer FETs, which is substantially lower than the measured 200 cm^2 V^{-1} s^{-1} of the bulk MoS_2.[7] The very low mobility is believed to be due to the charge disorder caused by unwanted chemical bonding and/or roughness at the interfaces. However, the use of other gate dielectric materials such as HfO_2 and Al_2O_3 by several research groups had demonstrated much higher mobility values.[11,12] However, the complicated process of exfoliating single-layer MoS_2 with an additional high-*k* dielectric layer may significantly limit its compatibility with commercial fabrication. Besides, the traditional mechanical exfoliation method lacks in the formation of large-scale SL and few-layer MoS_2 films, limiting its use for widespread applications. Therefore, the large-scale synthesis of high-quality single- or few-layer MoS_2 is still a challenge.

For synthesizing large-area MoS_2 thin films, several research groups attempted a wide range of methods, including thermal evaporation, van der Waal epitaxy (VDWE), sputtering, pulsed laser deposition (PLD), and electron beam evaporation (EBE).[13−16] However, most of these techniques have been reported to produce MoS_2 in morphologies other than layered (e.g., nanoparticles, nanorods, and nanotubes). This is mainly

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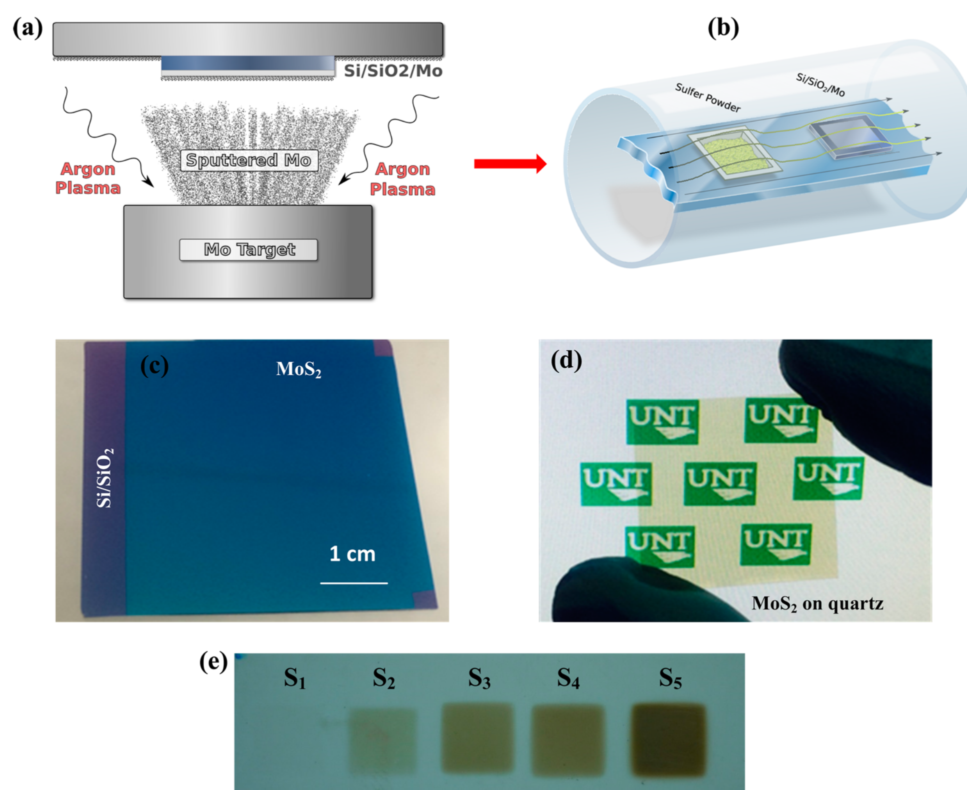

Figure 1. Schematic diagram of two-step (a) sputtering and (b) CVD method for the growth of MoS_2 thin films. Optical images of large-area MoS_2 growth on (c) Si/SiO_2 and (d) transparent substrate. (e) Optical contrast of MoS_2 films for samples S_1−S_5 shows different thicknesses.

due to the fact that such approaches produce many nucleation sites and the resultant film growth is initiated from these sites. Techniques like VDWE and molecular beam epitaxy (MBE), at very low vacuum and controlled deposition rates, can produce ordered 2D layered structures,[14,17] but they are rather expensive. Other methods have been studied to produce MoS_2, including liquid phase deposition, liquid exfoliation, laser thinning, solid state reactions, and hydrothermal methods, but they take several preparation processes and are useful only for the production of composites and hybrid dispersions.[18−20] So far, chemical vapor deposition has been demonstrated as the most practical method of synthesizing large-area and high-quality graphene, boron nitride, and 2D TMD nanosheets.[21,22] A direct growth of MoS_2 monolayers can be achieved on various substrates by using the vapor-phase reaction of MoO_3 and S powders in a CVD system. Najmaei et al.[23] synthesized MoS_2 atomic layers on Si/SiO_2 substrates by using this method and reported an average mobility and maximum current on/off ratio of 4.3 $cm^2\ V^{-1}\ s^{-1}$ and $\sim 10^6$, respectively. However, the main concern of this method is the formation of MoS_2 monolayer crystal flakes on the substrates rather than the formation of a continuous MoS_2 layer, and sometimes, the reaction normally leads to MoS_2 nanoparticles or nanorod structures with formation of byproducts like MoO_2 during the synthesis.[24,25] Zhan et al.[26] grew large-area MoS_2 films via e-beam evaporation and CVD methods and found a *p*-type conduction but with very poor mobility in the range of 0.004−0.04 $cm^2\ V^{-1}\ s^{-1}$. Recently, Yu et al.[27] developed a new method that precisely controls the number of MoS_2 layers over a large area by using $MoCl_5$ and sulfur as precursor materials in a CVD at high temperature. However, the field effect mobility of charge carriers in their device was found to be very low (0.003−0.03 $cm^2\ V^{-1}\ s^{-1}$). In considering the theoretical estimation that the energy band gap change of MoS_2 with thickness, it is, therefore, imperative to develop a suitable deposition method for the growth of thickness-modulated films while demonstrating high-quality, uniform, and continuous films over a large area exhibiting excellent electrical properties.

Here, we present a simple and scalable two-step sputtering−CVD reaction approach that can produce high-quality, large-scale, and thickness-modulated MoS_2 atomic layers on a Si/SiO_2 substrate. The presence of single layers over a 2″ wafer was confirmed by Raman mapping, AFM, and HRTEM images. Electrical measurements demonstrated a *p*-type semiconductor behavior with significantly high mobility and $I_{on/off}$ ratio as compared to exfoliated and other CVD grown MoS_2 films on silicon substrates. This method is compatible to the conventional semiconductor process and can be extended to other TMDs and arbitrary substrates by transferring MoS_2 layers, including flexible substrates for flexible electronic applications.

2. RESULTS AND DISCUSSION

Figure 1a,b illustrates the schematic diagram of our two-step synthesis method that involves the deposition of Mo films with different thicknesses on Si/SiO_2 substrates using magnetron sputtering, followed by their sulfurization in a CVD chamber. Figure 1c,d shows optical images of uniform and large-scale growth of MoS_2 films using our two-step sputtering−CVD method. Figure 1e shows the optical images of MoS_2 films with different thicknesses (S_1−S_5) grown on a transparent quartz substrate. The optical contrast in different samples clearly shows the variation in MoS_2 thickness. The number of atomic layers in MoS_2 thin films can be identified from measuring the thickness by an atomic force microscope (AFM). Figure 2a

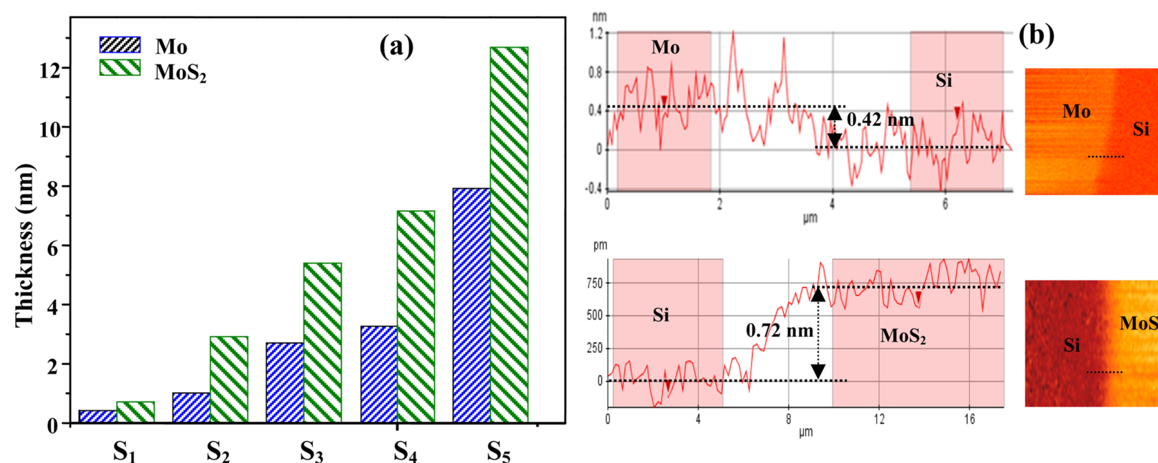

Figure 2. (a) Bar graph of Mo and MoS_2 film thickness for samples S_1–S_5. (b) AFM height profiles and images of a Mo and MoS_2 film on a Si/SiO_2 substrate (sample S_1).

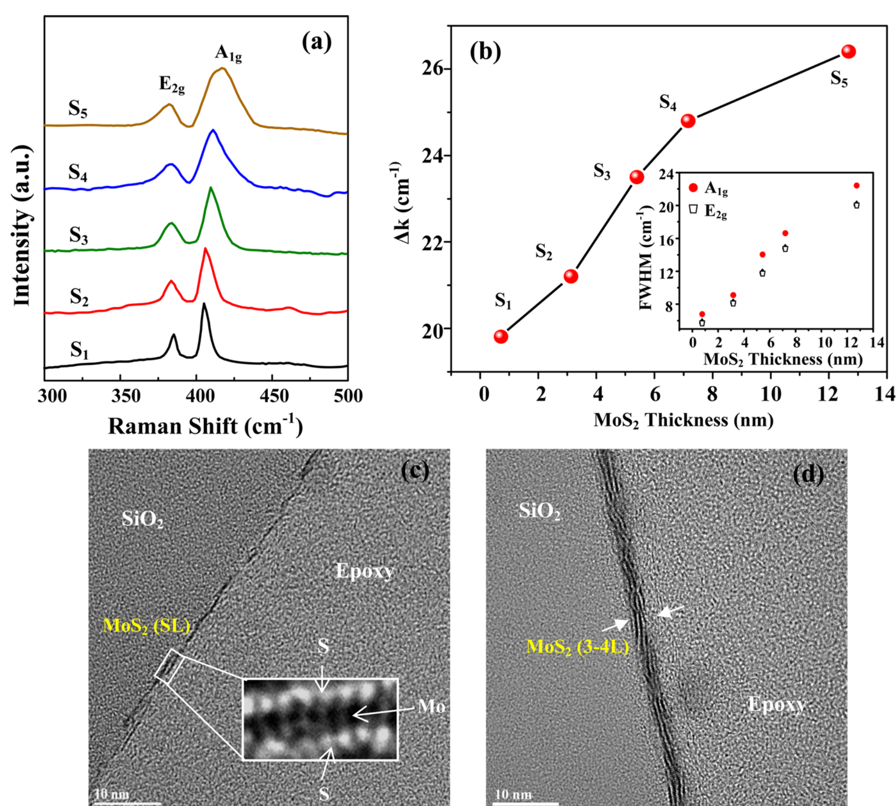

Figure 3. (a) Raman spectra of MoS_2 thin films corresponding to samples S_1–S_5. (b) Difference between the in-plane (E^1_{2g}) and out-of-plane (A_{1g}) Raman modes (Δk) with increasing MoS_2 film thickness: Inset shows the Raman peak FWHM of E^1_{2g} and A_{1g} modes. Cross-sectional HRTEM images of (c) sample S_1 (inset shows the SL MoS_2 structure) and (d) sample S_2.

shows the thickness bar chart for Mo and MoS_2 thin films corresponding to samples S_1–S_5. The thickness of MoS_2 films as estimated by AFM height profiles was found to be 0.72, 3.01, 5.40, 7.16, and 12.69 nm corresponding to samples S_1, S_2, S_3, S_4, and S_5, respectively. The cross-sectional height in Figure 2b reveals that the thickness of MoS_2 film for sample S_1 is ~0.72 nm, which typically corresponds to one atomic layer of MoS_2 based on previous reports for a monolayer MoS_2 on a Si/SiO_2 substrate.[28] It is now well-known that the difference between the in-plane (E^1_{2g}) and out-of-plane (A_{1g}) Raman modes (Δk) is an appropriate quantity to assign the number of MoS_2 layers on a variety of substrates.[29,30] Figure 3a shows the Raman spectra of MoS_2 films with different thicknesses, measured at 532 nm excitation laser line. For sample S_1, the two Raman characteristic bands at 405.2 and 385.5 cm^{-1} corresponding to A_{1g} and E^1_{2g} vibration modes show a peak frequency difference of 19.7 cm^{-1}, which evidences the existence of monolayer MoS_2.[26,27] The higher value of Δk as compared to their exfoliated counterparts could be related to crystalline imperfection due to smaller crystalline grains ranging from 20 to 80 nm in the as-synthesized thin film.[31] It is apparent from the Raman spectra of samples S_2–S_5 that the E_{2g} and A_{1g} peaks shift apart from each other with increasing MoS_2 thickness, which, in turn, increases the frequency difference (Δk) of the

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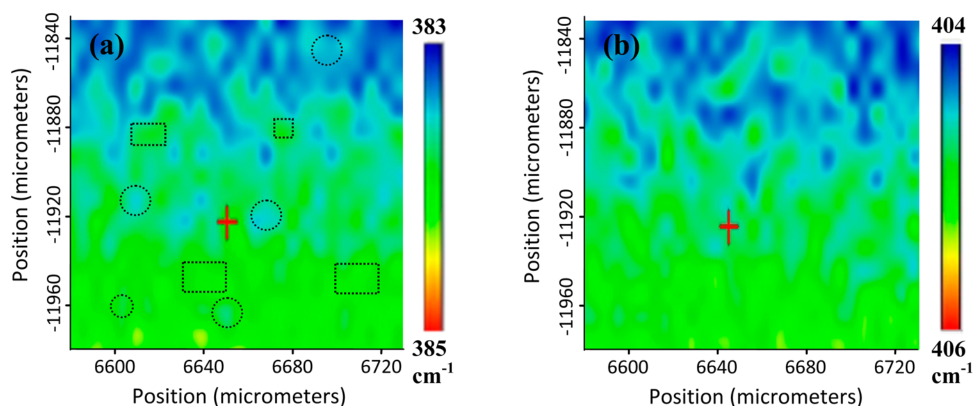

Figure 4. Raman mapping images of (a) E^1_{2g} and (b) A_{1g} frequencies for a 150 μm × 150 μm area for sample S_1.

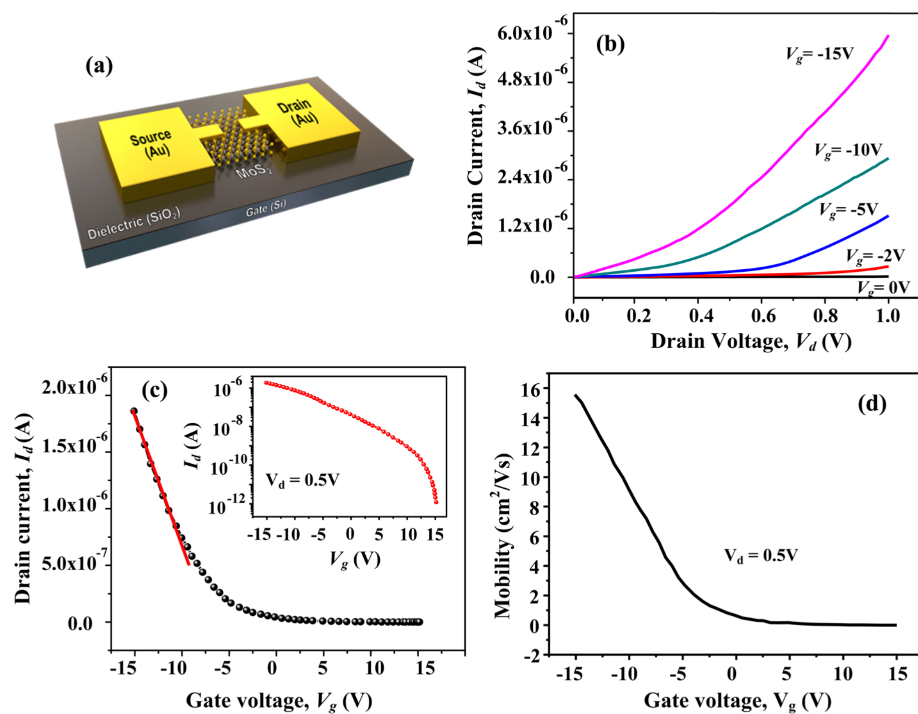

Figure 5. (a) 3D view of the MoS_2 FET. (b) Room-temperature output (I_d−V_d) characteristics for sample S_2 as a function of gate bias V_g from 0 to −15 V. (c) Drain-source current I_d as a function of back-gate voltage V_g at fixed V_d = 500 mV with linear fit of the data to calculate field effect mobility. Inset shows the I_d−V_g curve plotted in logarithmic scale as a function of back-gate voltage V_g at fixed V_d = 500 mV. (d) Range of field effect mobility (μ) as a function of gate voltage for sample S_2.

synthesized thin films (Figure 3b), consistent with what was observed on exfoliated MoS_2.[26,31] It is also worth noting that the full width at half-maximum (FWHM) of the Raman peaks increases with increasing MoS_2 thickness, as shown in the inset of Figure 3b. The lower value of FWHM in the case of samples S_1 and S_2 represents the high structural quality in our MoS_2 films.[32] To further confirm the quality and number of MoS_2 layers, HRTEM was performed, and Figure 3c,d shows the cross-sectional views of MoS_2 layers on Si/SiO_2 substrates for samples S_1 and S_2, respectively. The thickness of the MoS_2 layer extracted from HRTEM was found to be 0.69 ± 0.02 nm for sample S_1, which confirms the formation of a monolayer, whereas sample S_2 shows a clear stacking of 3−4 MoS_2 layers. Inset of Figure 3c clearly shows the structure and formation of SL MoS_2. The results obtained by HRTEM are found in well agreement with our AFM height profiles and Raman spectra. The formation of voids or discontinuity in SL MoS_2 layer (Figure 3c) could be attributed to very low deposition time for Mo atoms to reach substrate surface with sufficiently high energy.

It is difficult to obtain uniform single-layer (SL) MoS_2 over the entire substrate after sulfurization of deposited Mo films (S_1) for the reasons stated in the Introduction section of this paper. To ascertain the uniformity of SL MoS_2 for sample S_1, Raman mapping of E^1_{2g} and A_{1g} frequencies was collected over a wide area of 150 μm × 150 μm, as shown in Figure 4a,b, respectively. We noted that the average peak spacing between E^1_{2g} and A_{1g} calculated from the areas marked as dotted circles was found to be ~19.7 cm^{-1}, indicating the presence of monolayers, while the areas shown in rectangles exhibit an average peak spacing of ~21.2 cm^{-1}, which represents approximately two layers of MoS_2. In addition, our results are consistent with the Raman mapping analysis of Lee et al.[29] and Zhan et al.[26] that shows a blue shift for E^1_{2g} and a red shift for

Table 1. Comparison of Various MoS_2 FETs Fabricated on Si/SiO_2 Substrates

S. no.	method	field effect mobility ($cm^2\ V^{-1}\ s^{-1}$)	ON/OFF ratio	reference
1	**sputtering−CVD**	**12.24**	**1.56×10^6**	**this work**
2	CVD	0.02	$\sim 10^4$	44
3	CVD	0.003−0.03	$\sim 10^3$	27
4	thermolysis	6.0	$\sim 10^6$	45
5	CVD	4.3	6.0×10^6	23
6	exfoliated	1.5	$\sim 10^2$	46
7	exfoliated	3.0		9
8	e-beam−CVD	0.004−0.04		26
9	CVD	0.03−0.23	$\sim 10^5$	47
10	exfoliated	0.1−10	1×10^6	7
11	exfoliated	10−15	10^7	10
12	CVD	17	10^8	48

A_{1g} with the decrease in MoS_2 film thickness. The thickness variation for sample S_1 was in the range of 0.65−1.32 nm, as confirmed by AFM. Hence, by employing AFM, HRTEM, and Raman analyses, we confirmed the formation of single-layer MoS_2 over 2″ wafers with a uniform area of 10−15 μm^2, which is still a larger size than exfoliated MoS_2.[33−35] The defects observed in monolayer MoS_2 (sample S_1) could be attributed to the layer-and-island growth modes of Mo films.[36] However, the films were found to be uniform and continuous over an area of 2 in. for sample S_2 and S_3.

After the growth and characterization of the MoS_2 films with different thicknesses on Si/SiO_2 substrates, their electrical properties were evaluated by fabricating MoS_2 field effect transistor (FET) devices with 50 nm thick Au as source and drain electrodes, 300 nm thick SiO_2 served as the dielectric layer, while doped silicon was used as the back gate. Figure 5a shows the schematic view of the transistor. The electrical measurement on sample S_1 showed a very high resistance without any indication of FET behavior or gate biasing effect. It could be attributed to the large spatial constraints imposed by the substrates for very thin layers of MoS_2 film and discontinuity or void formation for sample S_1. It was observed that an increase in MoS_2 thickness up to 2.92 nm for sample S_2 results in large-area and uniform growth of 3−4 MoS_2 atomic layers exhibiting a good FET behavior with pronounced gate bias modulation. Figure 5b shows the typical output characteristics, i.e., drain current versus drain voltage (I_d−V_d) as a function of gate voltage varying from 0 to −15 V. It is evident from the figure that the I_d−V_d curve exhibits negligibly very low currents at zero gate voltage (V_g = 0), whereas a significant increase in drain current was observed with increasing gate voltage up to −15 V. Figure 5c shows the dependence of drain current on the back-gate voltage (I_d−V_g) at a drain-source voltage of 0.5 V for sample S_2. The lack of drain current saturation in the transfer characteristics (I_d−V_g) of sample S_2 could be attributed to the presence of a thick SiO_2 back-gate dielectric. It is worth to note that the transfer characteristic of sample S_2 represents a *p*-type behavior differently from the naturally grown MoS_2 crystal that is an *n*-type semiconductor.[9,37] The *p*-type behavior in our layered MoS_2 could be due to the presence of localized trap states that are expected to present at the interface of the Si/SiO_2 substrate and MoS_2 film, which tends to relocate the Fermi level of the SiO_2/MoS_2 system just below the valence band maxima, making the system a *p*-type semiconductor.[38] The trap states might have originated from the immobile ionic charges, SiO_2 surface oxygen dangling bonds or foreign impurities presented at the SiO_2/MoS_2 interface during MoS_2 synthesis.[39] The defects present at the SiO_2 and MoS_2 interface could also be due to the Mo diffusion into SiO_2 when it was sulfurized in the CVD furnace at the high temperature of 600 °C. There are several other reports showing the *p*-type conductivities in ultrathin MoS_2 layers deposited on SiO_2. Zhan et al.[26] also reported a *p*-type behavior in CVD grown MoS_2 layers on Si/SiO_2 substrates. Zeng et al.[28] fabricated single-layer MoS_2 by a lithiation process and observed a *p*-type doping on the Si/SiO_2 substrate. There may be a possibility of doping by creating Mo and/or S vacancies in MoS_2 layers and introducing dopants on MoS_2 films,[40,41] but those vacancies might be vulnerable to deep trap states in the MoS_2 band gap.[42] Therefore, the conducting behavior of MoS_2 seems to depend on the experimental details and substrate conditions; hence, more detailed experimental and theoretical studies should be done to understand the origin of current polarity (*n*- or *p*-type) in 2D MoS_2 thin films.

The drain current I_d for sample S_2 was replotted on a logarithmic scale as a function of V_g (inset of Figure 5c). At V_g = +15 V, the MoS_2 channel of the FET was found to be pinched off with an OFF-state $I_d \sim 1.18 \times 10^{-12}$ A while the ON-state current I_d at V_g = −15 V was approximately 1.86×10^{-6} A, yielding a corresponding current on/off ratio $\sim 1.57 \times 10^6$. The field effect mobility of this FET was calculated by using the formula[43]

$$\mu = \left(-\frac{L}{WC_{ox}}\right)\left(\frac{1}{V_d}\frac{\Delta I_d}{\Delta V_g}\right) \quad (1)$$

where $\Delta I_d/\Delta V_g$ was determined from the slope of a linear fit of the data from the I_d−V_g curve. V_d: drain-source voltage (0.5 V); L: gate length (10 μm); W: device width (30 μm); $C_{ox} = \varepsilon_o\varepsilon_r/d$ is the gate insulator capacitance, for SiO_2, $\varepsilon_o = 8.854 \times 10^{-12}$ F/m, ε_r = 3.9, thickness of dielectric, d = 300 nm. The average value of field effect mobility was determined to be 12.24 ± 0.741 $cm^2\ V^{-1}\ s^{-1}$. Figure 5d shows the range of field effect mobility values as a function of gate voltage for sample S_2. Table 1 compares the $I_{on/off}$ ratio and field effect mobility of our two-step grown MoS_2 device with previously reported mechanically exfoliated and CVD grown MoS_2 FETs on Si/SiO_2 substrates.[7,9,10,23,26,27,44−48] A significant improvement in the transistor parameters can be noticed in our *p*-type MoS_2 FETs as compared to other research groups' devices. It is worth to note that our result from polycrystalline MoS_2 film is almost as good as that of single crystal MoS_2.[48] Also, the field effect mobility in our MoS_2 FETs is much higher than that in the commercially available thin film FETs based on amorphous

silicon (a-Si) and organic materials.[49−52] A similar behavior of the output (I_d−V_d) and transfer (I_d−V_g) characteristics exhibiting *p*-type conduction was observed for sample S_3. The value of the $I_{on/off}$ ratio and average field effect mobility for sample S_3 were found to be 5.7×10^4 and 0.44 ± 0.062 cm^2 V^{-1} s^{-1}, respectively. With a further increase in MoS_2 film thickness for sample S_4 (7.16 nm) and S_5 (12.69 nm), a significant drop in MoS_2 resistance showing a metallic type behavior was observed in the FET characterization. We believe that 100% Mo was not converted to MoS_2 during sulfurization at higher thickness of Mo films. The theoretical MoS_2 thickness was calculated by considering a change in lattice parameter of Mo (∼3.147 Å) to MoS_2 (∼12.29 Å) by sulfurization. The thickness of MoS_2 corresponding to S_1, S_2, S_3, S_4, and S_5 was estimated to be 1.11, 4.18, 6.44, 14.11, and 34.99 nm, respectively. It can be observed that the theoretical and experimental values (Figure 2) of MoS_2 thickness were in agreement up to sample S_3, but there was a large deviation when Mo film thickness increases for sample S_4 and S_5 that could be attributed to the partial sulfurization of Mo at higher thicknesses.

3. CONCLUSIONS

In conclusion, we succeeded in fabricating large-area, thickness-modulated MoS_2, varying from single- to few-layer MoS_2 films on Si/SiO_2 substrates using a combination of magnetron sputtering, followed by chemical vapor deposition. Raman spectra, AFM height measurement data, and HRTEM images demonstrated the presence of single-layer MoS_2 over an area of 2 in. with the domain size of 10−15 μm^2. The electric measurement for the bottom-gate transistor shows a dominant *p*-type semiconductor behavior with the high current on/off ratio of 1.57×10^6 and a high field effect mobility of 12.24 ± 0.741 cm^2 V^{-1} s^{-1}. Our results demonstrated an important step toward device fabrication with controlled MoS_2 synthesis. These results suggest that large-area growth of MoS_2 atomic layers with *p*-type conduction would increase the compatibility and integration of these TMDs in current nano- and micro-*p*-FET applications and also open avenues in flexible and high-temperature radiation hard electronic and optoelectronic devices.

4. EXPERIMENTAL METHODS

Sample Growth. In our two-step method, the first step involves the synthesis of Mo thin films at room temperature on (100) oriented N-type (as doped, resistivity < 0.005 Ω.cm) silicon substrates coated with a 300 nm thick SiO_2 layer. The deposition time was varied from 4 to 180 s to obtain a batch of Mo films with increasing thicknesses. A high-purity (99.99%) Mo metal target of 50 mm in diameter was used for sputtering Mo thin films. The substrates were initially cleaned thoroughly with acetone in an ultrasonic bath, followed by cleaning in ethanol, methanol, and DI water. The substrates were fixed on the heater, and the chamber was evacuated to a vacuum level of 10^{-7} Torr. Before every sputtering run, the target was presputtered for 5 min to ascertain the same state of Mo target for each sample. In the second step, magnetron sputtered Si/SiO_2/Mo films were subsequently placed in a low-pressure chemical vapor deposition (LPCVD) system (Graphene Square CVD) equipped with a 4 in. diameter quartz tube furnace. A ceramic boat containing pure sulfur (∼1 gm, Sigma-Aldrich) was placed in the upstream of quartz tube. Argon was used as a carrier gas to convey sulfur vapor species to the downstream Mo films. The tube was pumped down to a pressure of 10^{-3} Torr and flushed with Ar gas repeatedly to guarantee a favorable growth atmosphere. In the flow atmosphere of 200 sccm Ar with a chamber pressure of 5 Torr, the furnace was heated to 600 °C at the center zone in 30 min. After 60 min, the furnace was cooled down naturally to room temperature. The samples S_1, S_2, S_3, S_4, and S_5 corresponds to MoS_2 films converted for Mo films deposited at different sputtering times of 4, 10, 30, 60, and 180 s, respectively.

Characterization. The height measurement of Mo and MoS_2 films was performed by an AFM (Parks NX-10) system. Raman spectra of MoS_2 thin films were collected in an Almega XR Raman spectrometer equipped with an Olympus BX51 microscope with motorized stage, mapping capabilities, and spatial resolution down to 1 μm, and the wavelength of the laser is 532 nm. The MoS_2 films were characterized by a TECNAI F20 S-Twin (FEI Co, Netherland) transmission electron microscope (TEM) operating at an accelerating voltage of 120 kV equipped with energy-dispersive spectroscopy (EDS). The cross section of the TEM sample was lifted-out with a Quanta 3D dual-focused ion beam (FIB) on the Mo half grid for quantitative EDS analysis. The electrical measurements were performed at room temperature using an Agilent B2912A precision source/measure unit (2 ch, 10 fA, 210 V, 3A DC/10.5A pulse) connected to a probe station with 20 μm size tungsten probes. The FET test on each sample was performed at 15 different regions in large-area films to obtain the statistics of the electrical performance. All electrical measurements on MoS_2 devices were performed in vacuum in order to isolate the effect of ambient oxygen and water.

AUTHOR INFORMATION

Corresponding Author

*E-mail: wonbong.choi@unt.edu. Telephone: +1-940-369-7673 (W.C.).

Notes

The authors declare no competing financial interest.

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